Solutions - Homework 1

(Due date: January 17th @ 5:30 pm)

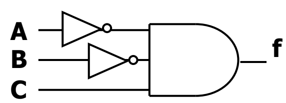
Presentation and clarity are very important!

PROBLEM 1 (27 PTS)

a) Simplify the following functions using ONLY Boolean Algebra Theorems. For each resulting simplified function, sketch the logic circuit using AND, OR, XOR, and NOT gates. (14 pts)

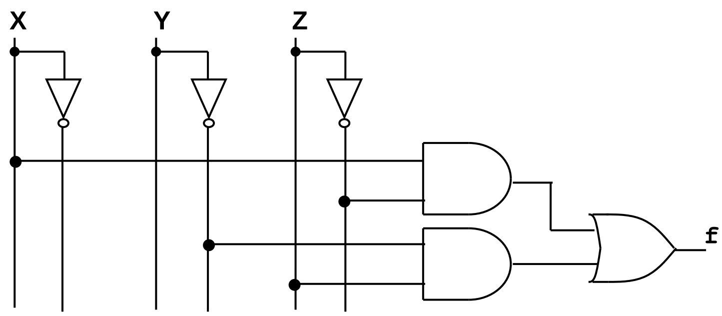
- ✓ $F = \overline{\bar{A}(B+\bar{C})+A}$
- ✓ $F(X,Y,Z) = \prod(M_2, M_4, M_6, M_7)$
- ✓ $F = (Z+X)(\bar{Z}+\bar{Y})(\bar{Y}+X)$
- ✓ $F = \overline{(X+Y)}Z + \bar{X}\bar{Y}\bar{Z}$

✓ $F = \overline{\bar{A}(B+\bar{C})+A} = \overline{\bar{A}(B+\bar{C})}.\bar{A} = \left(A+\overline{B+\bar{C}}\right).\bar{A} = \left(\overline{B+\bar{C}}\right).\bar{A} = \bar{A}\bar{B}C$



✓ $F = (Z+X)(\bar{Z}+\bar{Y})(X+\bar{Y}) = (Z+X)(\bar{Z}+\bar{Y})$ (Consensus Theorem)

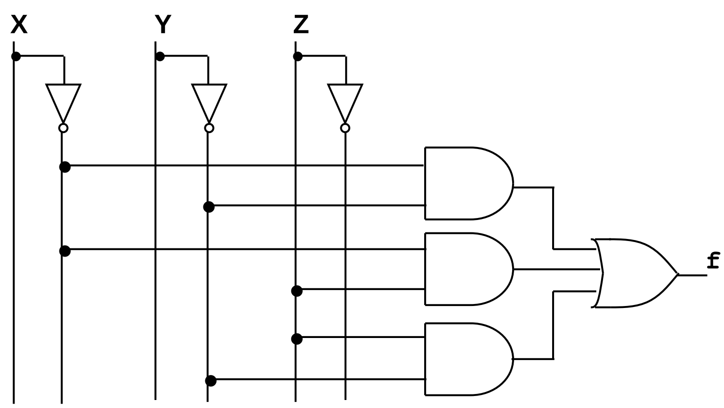
$(Z+X)(\bar{Z}+\bar{Y}) = Z\bar{Y} + \bar{Z}X + X\bar{Y} = Z\bar{Y} + \bar{Z}X$ (Consensus Theorem)



✓ $F(X,Y,Z) = \prod(M_2,M_4,M_6,M_7) = \sum(m_0,m_1,m_3,m_5) = \bar{X}\bar{Y}\bar{Z} + \bar{X}\bar{Y}Z + \bar{X}YZ + X\bar{Y}Z = \bar{X}\bar{Y} + \bar{X}YZ + X\bar{Y}Z$

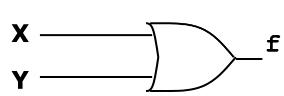
$F(X,Y,Z) = \bar{X}\bar{Y} + \bar{X}YZ + X\bar{Y}Z = \bar{X}(\bar{Y}+YZ) + X\bar{Y}Z = \bar{X}(\bar{Y}+Z) + X\bar{Y}Z = \bar{X}\bar{Y} + \bar{X}Z + X\bar{Y}Z$

$F(X,Y,Z) = \bar{X}\bar{Y} + \bar{X}Z + X\bar{Y}Z = \bar{X}\bar{Y} + Z(\bar{X}+X\bar{Y}) = \bar{X}\bar{Y} + Z(\bar{X}+\bar{Y}) = \bar{X}\bar{Y} + Z\bar{X} + Z\bar{Y}$



✓ $F = \overline{\overline{(X+Y)}Z + \bar{X}\bar{Y}\bar{Z}} = \overline{\overline{(X+Y)}Z}.\overline{\bar{X}\bar{Y}\bar{Z}} = (X+Y+\bar{Z})(X+Y+Z) = (A+\bar{Z})(A+Z), A = X+Y$

$F = (A+\bar{Z})(A+Z) = A = X+Y$



b) Using ONLY Boolean Algebra Theorems, demonstrate that the XOR operation is associative: (5 pts)

$$(a \oplus b) \oplus c = a \oplus (b \oplus c) = b \oplus (a \oplus c)$$

$(a \oplus b) \oplus c = (a\bar{b} + \bar{a}b) \oplus c = (\overline{a\bar{b} + \bar{a}b})c + (a\bar{b} + \bar{a}b)\bar{c} = (ab + \bar{a}\bar{b})c + (a\bar{b} + \bar{a}b)\bar{c} = abc + \bar{a}\bar{b}c + a\bar{b}\bar{c} + \bar{a}b\bar{c} = \sum m(7,1,4,2)$.

$a \oplus (b \oplus c) = a \oplus (b\bar{c} + \bar{b}c) = a(bc + \bar{b}\bar{c}) + \bar{a}(b\bar{c} + \bar{b}c) = abc + a\bar{b}\bar{c} + \bar{a}b\bar{c} + \bar{a}\bar{b}c = \sum m(7,4,2,1)$.

$b \oplus (a \oplus c) = (a \oplus c) \oplus b = (a\bar{c} + \bar{a}c) \oplus b = (ac + \bar{a}\bar{c})b + (a\bar{c} + \bar{a}c)\bar{b} = acb + \bar{a}\bar{c}b + a\bar{c}\bar{b} + \bar{a}c\bar{b} = \sum m(7,2,4,1)$.

* Note that $x \oplus y = y \oplus x$

c) For the following Truth table with two outputs: (8 pts)
- Provide the Boolean functions using the Canonical Sum of Products (SOP), and Product of Sums (POS).
- Express the Boolean functions using the minterms and maxterms representations.
- Sketch the logic circuits as Canonical Sum of Products and Product of Sums.

x	y	z	f_1	f_2
0	0	0	0	0
0	0	1	1	0
0	1	0	1	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	1
1	1	1	0	1

Sum of Products

$f_1 = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + \bar{X}YZ + X\bar{Y}\bar{Z} + XY\bar{Z}$

$f_2 = \bar{X}Y\bar{Z} + \bar{X}YZ + X\bar{Y}Z + XY\bar{Z} + XYZ$

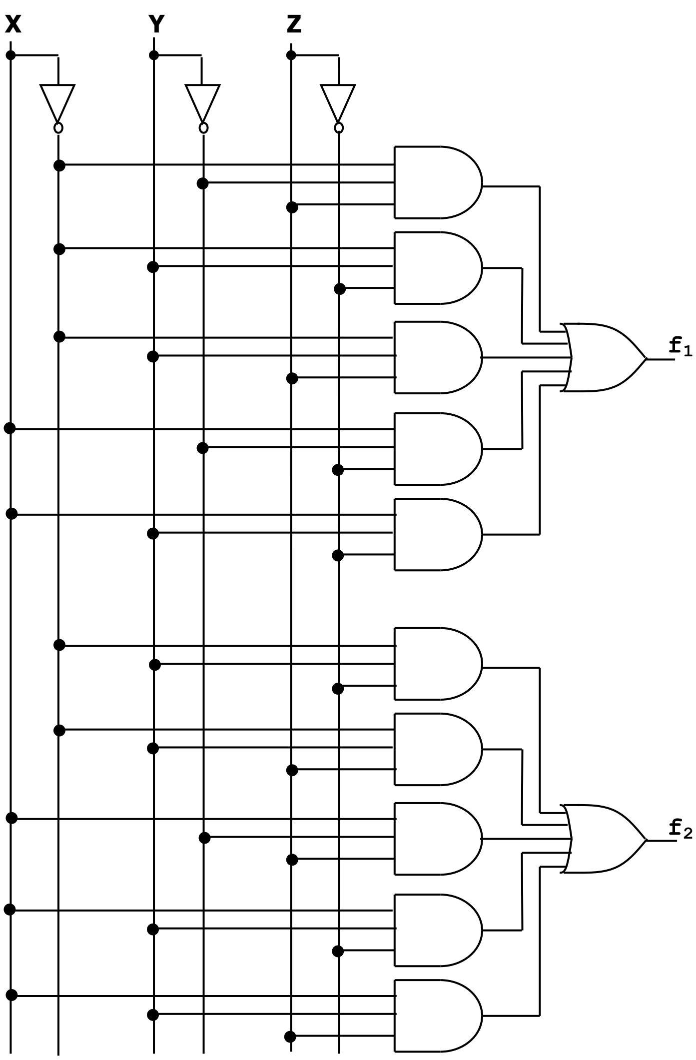
Product of Sums

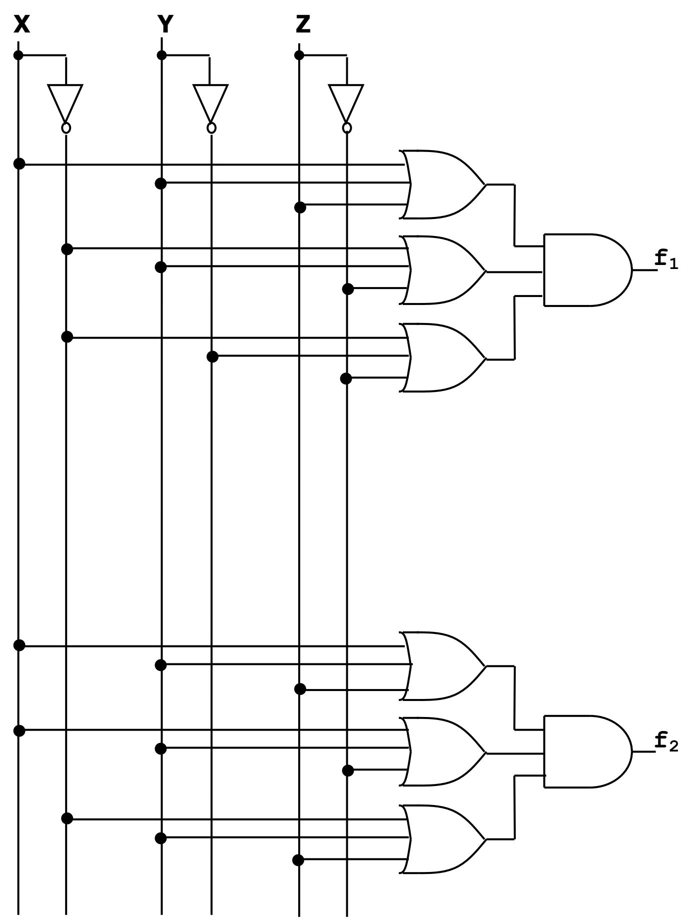
$f_1 = (X + Y + Z)(\bar{X} + Y + \bar{Z})(\bar{X} + \bar{Y} + \bar{Z})$

$f_2 = (X + Y + Z)(X + Y + \bar{Z})(\bar{X} + Y + Z)$

Minterms and maxterms: $f_1 = \sum(m_1, m_2, m_3, m_4, m_6) = \prod(M_0, M_5, M_7)$.

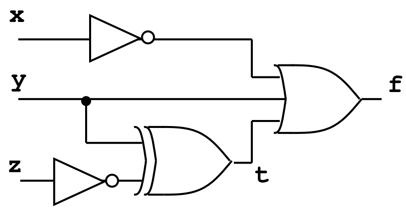
$f_2 = \sum(m_2, m_3, m_5, m_6, m_7) = \prod(M_0, M_1, M_4)$.





PROBLEM 2 (25 PTS)

a) Construct the truth table describing the output of the following circuit and write the simplified Boolean equation (6 pts).

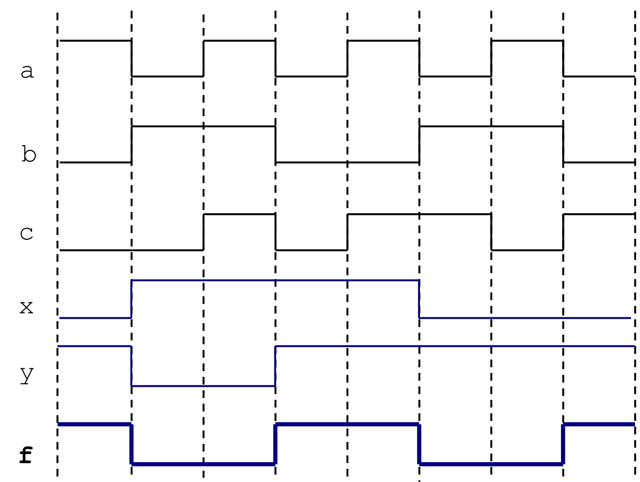


x	y	z	t	f
0	0	0	1	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	1	1
1	0	1	0	0
1	1	0	0	1
1	1	1	1	1

$f = \bar{x} + y + \bar{z}$

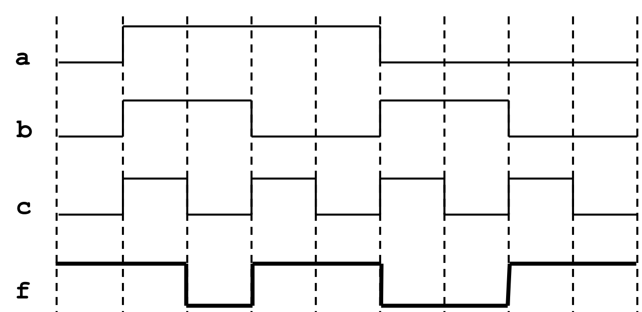
b) Complete the timing diagram of the logic circuit whose VHDL description is shown below: (6 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( a, b, c: in std_logic;
         f: out std_logic);
end circ;

architecture struct of circ is
  signal x, y: std_logic;

begin
  x <= a xor (not c);
  y <= x nand b;
  f <= y and (not b);
end struct;
```



c) The following is the timing diagram of a logic circuit with 3 inputs. Sketch the logic circuit that generates this waveform. Then, complete the VHDL code. (8 pts)

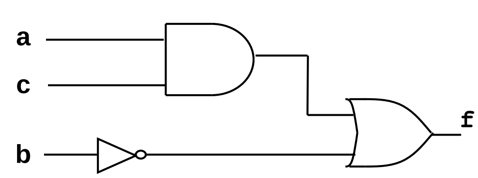
```
library ieee;
use ieee.std_logic_1164.all;

entity wav is
  port ( a, b, c: in std_logic;
               f: out std_logic);
end wav;

architecture struct of wav is

begin
   f <= not(b) or (a and c);
end struct;
```



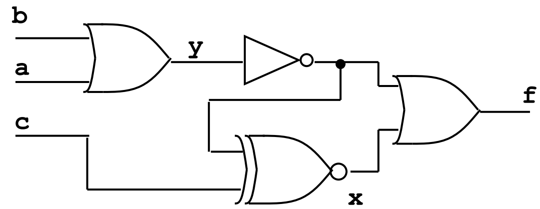
a	b	c	f
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

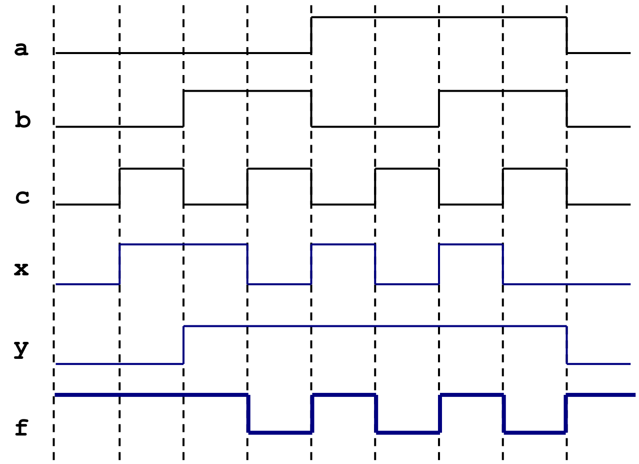
c \ ab	00	01	11	10
0	1	0	0	1
1	1	0	1	1

$f = \bar{b} + ac = \bar{b} + ac$



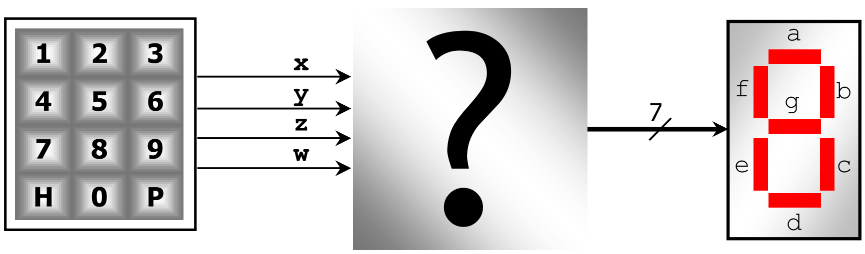
d) Complete the timing diagram of the following circuit: (5 pts)



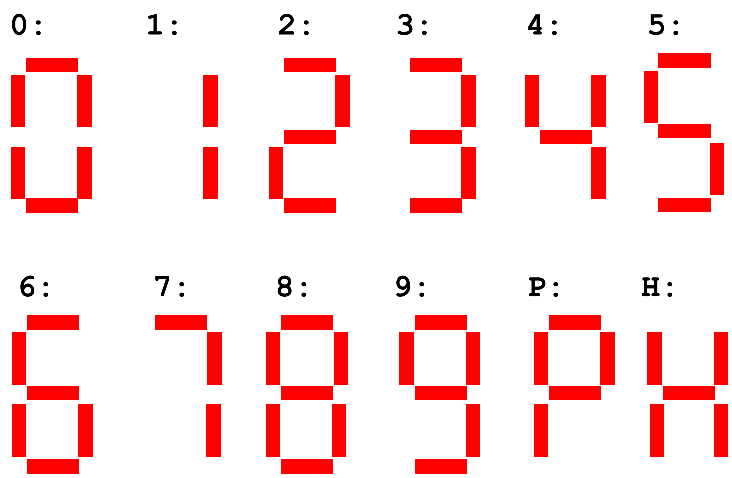


PROBLEM 3 (25 PTS)

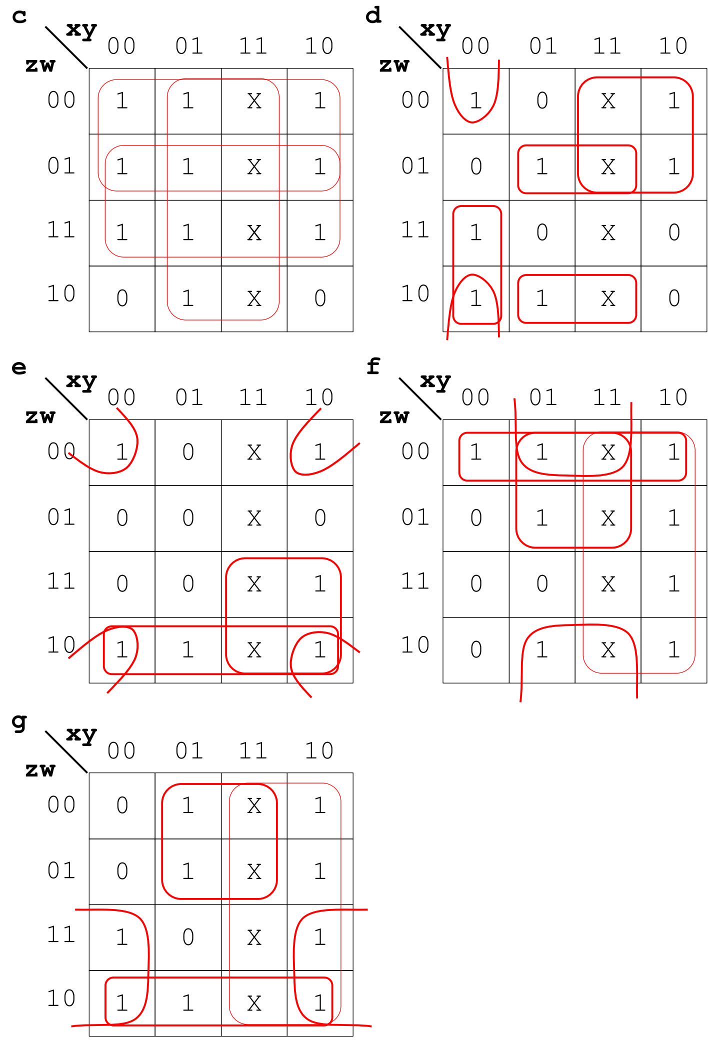
- A numeric keypad produces a 4-bit code as shown below. We want to design a logic circuit that converts each 4-bit code to a 7-segment code, where each segment is an LED: A LED is ON if it is given a logic '1'. A LED is OFF if it is given a logic '0'.
  - ✓ Complete the truth table for each output (a, b, c, d, e, f, g).
  - ✓ Provide the simplified expression for each output (a, b, c, d, e, f, g). Use Karnaugh maps for c, d, e, f, g and the Quine-McCluskey algorithm for a, b. Note: It is safe to assume that the codes `1100` to `1111` will not be produced by the keypad.



Value	X Y Z W	a b c d e f g
0	0 0 0 0	
1	0 0 0 1	
2	0 0 1 0	
3	0 0 1 1	
4	0 1 0 0	
5	0 1 0 1	
6	0 1 1 0	
7	0 1 1 1	
8	1 0 0 0	
9	1 0 0 1	1 1 1 1 0 1 1
P	1 0 1 0	
H	1 0 1 1	
	1 1 0 0	
	1 1 0 1	
	1 1 1 0	
	1 1 1 1	



Value	X	Y	Z	W	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
P	1	0	1	0	1	1	0	0	1	1	1
H	1	0	1	1	0	1	1	0	1	1	1
	1	1	0	0	X	X	X	X	X	X	X
	1	1	0	1	X	X	X	X	X	X	X
	1	1	1	0	X	X	X	X	X	X	X
	1	1	1	1	X	X	X	X	X	X	X



$c = y + \bar{z} + w$
$d = x\bar{z} + \bar{x}\bar{y}\bar{w} + \bar{x}\bar{y}z + \bar{z}wy + z\bar{w}y$
$e = \bar{w}\bar{y} + z\bar{w} + xz$
$f = x + \bar{z}\bar{w} + y\bar{z} + y\bar{w}$
$g = x + z\bar{w} + y\bar{z} + \bar{y}z$

- $a = \sum m(0,2,3,5,6,7,8,9,10) + \sum d(12,13,14,15)$.
  Too many minterms. We better optimize: $\bar{a} = \sum m(1,4,11) + \sum d(12,13,14,15)$

Number of ones	4-literal implicants	3-literal implicants	2-literal implicants	1-literal implicants
1	**m_1 = 0001** m_4 = 0100 ✓	**$m_{4,12}$ = -100**		
2	m_{12}= 1100 ✓	$m_{12,13}$ = 110- ✓ $m_{12,14}$ = 11-0 ✓	**$m_{12,13,14,15}$ = 11--** ~~$m_{12,14,13,15}$ = 11--~~ ✓	
3	m_{11}= 1011 ✓ m_{13}= 1101 ✓ m_{14}= 1110 ✓	$m_{13,15}$ = 11-1 ✓ $m_{14,15}$ = 111- ✓ **$m_{11,15}$ = 1-11**		
4	m_{15}= 1111 ✓			

$\bar{a} = \bar{x}\bar{y}\bar{z}w + y\bar{z}\bar{w} + xzw + xy$

Prime Implicants		Minterms		
		1	4	11
m_1	$\bar{x}\bar{y}\bar{z}w$	**X**		
$m_{4,12}$	$y\bar{z}\bar{w}$		**X**	
$m_{11,15}$	xzw			**X**
$m_{12,13,14,15}$	xy			

$\bar{a} = \bar{x}\bar{y}\bar{z}w + y\bar{z}\bar{w} + xzw \Rightarrow$ $a = (x + y + z + \bar{w})(\bar{y} + z + w)(\bar{x} + \bar{z} + \bar{w})$

- $b = \sum m(0,1,2,3,4,7,8,9,10,11) + \sum d(12,13,14,15)$.
  Too many minterms. We better optimize: $\bar{b} = \sum m(5,6) + \sum d(12,13,14,15)$

Number of ones	4-literal implicants	3-literal implicants	2-literal implicants	1-literal implicants
2	m_5 = 0101 ✓ m_6 = 0110 ✓ m_{12}= 1100 ✓	**$m_{5,13}$ = -101** **$m_{6,14}$ = -110** $m_{12,13}$ = 110- ✓ $m_{12,14}$ = 11-0 ✓	**$m_{12,13,14,15}$ = 11--** ~~$m_{12,14,13,15}$ = 11-- ✓~~	
3	m_{13}= 1101 ✓ m_{14}= 1110 ✓	$m_{13,15}$ = 11-1 ✓ $m_{14,15}$ = 111- ✓		
4	m_{15}= 1111 ✓			

$\bar{b} = \bar{x}\bar{y}\bar{z}w + y\bar{z}\bar{w} + xzw + xy$

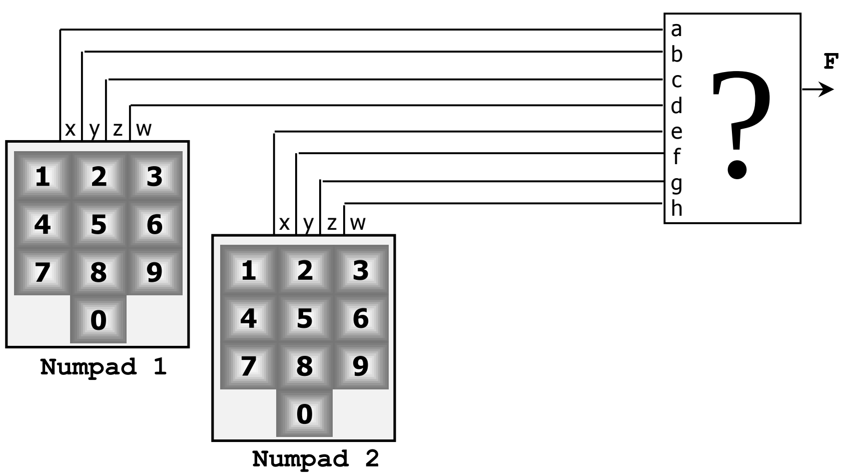
Prime Implicants		Minterms 5	Minterms 6
$m_{5,13}$	$y\bar{z}w$	**X**	
$m_{6,14}$	$yz\bar{w}$		**X**
$m_{12,13,14,15}$	xy		

$\bar{b} = y\bar{z}w + yz\bar{w} \quad \Rightarrow \quad b = (\bar{y} + z + \bar{w})(\bar{y} + \bar{z} + w)$

PROBLEM 4 (12 PTS)

- Design a logic circuit (simplify your circuit) that opens a lock ($f = 1$) whenever the user presses the correct number on each numpad (numpad 1: **7**, numpad2: **2**). The numpad encodes each decimal number using BCD encoding (see figure). We expect that the 4-bit groups generated by each numpad be in the range from 0000 to 1001. Note that the values from 1010 to 1111 are assumed not to occur.
  Suggestion: Create two circuits: one that verifies the first number (**7**), and another that verifies the second number (**2**). Then perform the AND operation on the two outputs. This avoids creating a truth table with 8 inputs.

BCD code x	y	z	w	Number pressed
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9



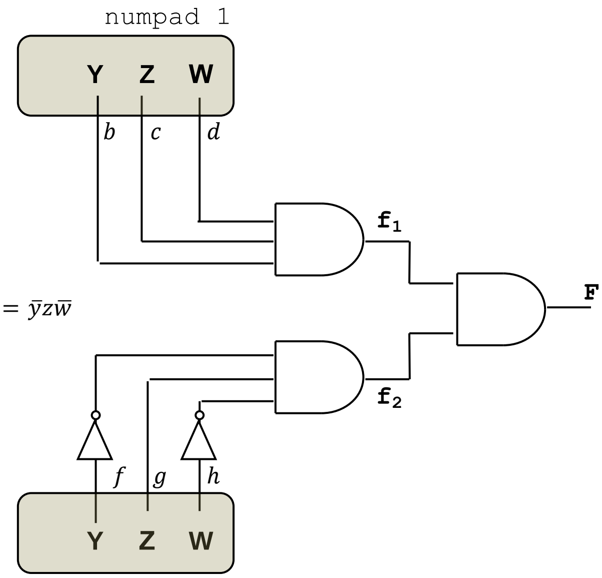
x	y	z	w	f_1	f_2
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	X	X
1	0	1	1	X	X
1	1	0	0	X	X
1	1	0	1	X	X
1	1	1	0	X	X
1	1	1	1	X	X

zw \ xy	00	01	11	10
00	0	0	X	0
01	0	0	X	0
11	0	1	X	X
10	0	0	X	X

$f_1 = yzw$

zw \ xy	00	01	11	10
00	0	0	X	0
01	0	0	X	0
11	0	0	X	X
10	1	0	X	X

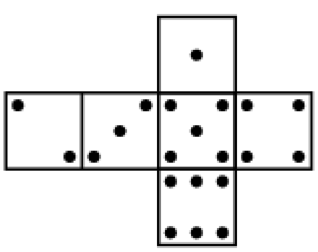
$f_2 = \bar{y}z\bar{w}$

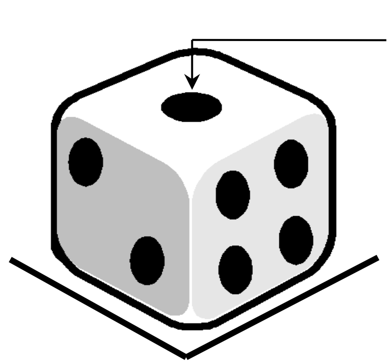


$F = bcd\bar{f}g\bar{h} = (bcd)(\bar{f}g\bar{h})$

PROBLEM 5 (11 PTS)

- The following die has a sensor on each side. Whenever a side rests on a surface, the sensor on that side generates a logic '1' (transmitted wirelessly to a controller); otherwise, it generates a '0'. The sensors outputs are named S1, S2, S3, S4, S5, S6.
- We want to design a circuit that reads the state of the 6 sensors and outputs a 3-bit value L representing the decimal value (unsigned integer) of the opposite side (upper surface). The output L is connected to 3 LEDs: A LED ON is represented by a logic '1', while the LED OFF is represented by '0'. For example, in the figure below:
  - ✓ The resting side has six dots. This means that the state of the sensors is S6=1, S5=0, S4=0, S3=0, S2=0, S1=0.
  - ✓ The opposite side (upper surface) has one dot representing the decimal number '**1**'. Thus, the output L must be 001.
- Under normal operation, we expect only one sensor activated at a time. However, due to a variety of problems, we might have the following cases:
  - ✓ Two or more sensors produce a '1' at the same time: Here, the state of the LEDs must be 000.
  - ✓ No sensor produces a '1': In this case, the state of the LEDs must be 000.
- Using the state of the sensors as inputs, provide the Boolean expression for each LED: L_2, L_1, L_0. First, build the truth table where the inputs are S6-S1 and the outputs are L_2-L_0.

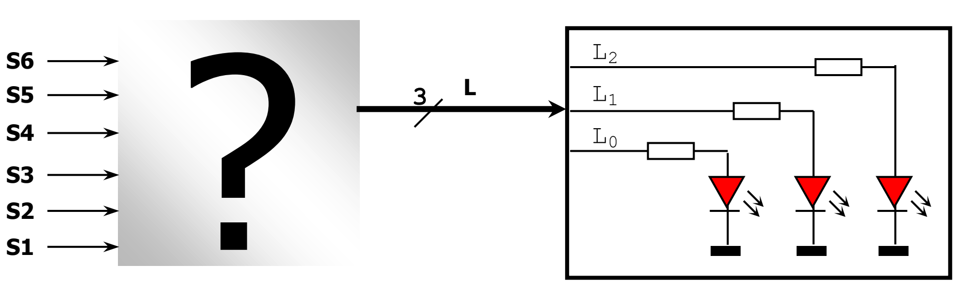




Resulting number: 1

State of Sensors

S6	S5	S4	S3	S2	S1
1	0	0	0	0	0



L_2	L_1	L_0	Number
0	0	0	-
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	-

S1	S2	S3	S4	S5	S6	L_2	L_1	L_0	Number
0	0	0	0	0	0	0	0	0	-
0	0	0	0	0	1	0	0	1	1
0	0	0	0	1	0	0	1	0	2
0	0	0	1	0	0	0	1	1	3
0	0	1	0	0	0	1	0	0	4
0	1	0	0	0	0	1	0	1	5
1	0	0	0	0	0	1	1	0	6
					...	0	0	0	-

$$L_2 = \overline{S1}\,\overline{S2}S3\overline{S4}\,\overline{S5}\,\overline{S6} + \overline{S1}S2\overline{S3}\overline{S4}\,\overline{S5}\,\overline{S6} + S1\overline{S2}\,\overline{S3}\,\overline{S4}\,\overline{S5}\,\overline{S6}$$

$$L_1 = \overline{S1}\,\overline{S2}\,\overline{S3}\,\overline{S4}S5\overline{S6} + \overline{S1}\,\overline{S2}\,\overline{S3}S4\overline{S5}\,\overline{S6} + S1\overline{S2}\,\overline{S3}\,\overline{S4}\,\overline{S5}\,\overline{S6}$$

$$L_0 = \overline{S1}\,\overline{S2}\,\overline{S3}\,\overline{S4}\,\overline{S5}S6 + \overline{S1}\overline{S2}\overline{S3}S4\overline{S5}\,\overline{S6} + \overline{S1}S2\overline{S3}\,\overline{S4}\,\overline{S5}\,\overline{S6}$$